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Voltage Sag Mitigation in Utility Connected System Using Current Source Converter Based D-STATCOM

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Abstract— This **paper discusses the implementation of current source converter based distribution type static synchronous compensator. For eliminating the lower order harmonics, the power semiconductors are switched by pulse width modulation technique. Current source converter, input filter, dc link reactor are combined to design the proposed CSC based STATCOM. Since the STATCOM is a current injection device, the performance of the device is improved by a current-source converter (CSC) combination. So a controllable current is generated at the output terminals of the device. Filter circuit at the input terminal is designed to eliminate the higher order harmonics. The proposed D- STATCOM is simulated and the results are validated using MATLAB.**

***Index Terms*—Static VAR Compensator, STATCOM, current source converter (CSC), voltage source converter (VSC), FACTS.**

I. Introduction

A static synchronous compensator (STATCOM) is an imperative member in FACTS Controllers. STATCOM is a switching power converter based static volt-ampere reactive (VAR) compensator. The capacitive and inductive output current of the circuit is controllable independent of the ac system voltage [1]. STATCOM has been replacing conventional SVCs gradually due to its better operational characteristics. Power factor correction, harmonics filtering, flicker compensation, and load balancing in the distribution side of a power system network are performed with Distribution type static synchronous compensator [2]. In a D-STATCOM, a voltage source converter (VSC) with a capacitor in the dc link or series reactors on the ac side is employed. A current-source converter (CSC) having a reactor in the dc link and shunt -connected capacitors on the ac side also employed for the compensating techniques. So the proposed CSC based D-STATCOM is the advanced choice for mitigating the voltage sag problems.

II. Current Source Converter (CSC)

The circuit diagram of current source converter is shown in Fig 1. It consists of six fully controllable power semiconductor switches (S1, S2, S3, S4, S5, S6). It has unidirectional current carrying and bipolar voltage blocking capabilities.

A dc -link reactor is used in the dc-link as an energy storage element. The equivalent circuit of dc link reactor is designed with series connection of dc-link inductance L_{dc} and its internal resistance R_{dc} [4]-[5]. Dc-link current I_{dc} becomes nearly constant. Based on pre-specified switching pattern, the switching of power semiconductors are carried out. So, almost constant dc-link current in the steady state is replicated at the ac lines of the CSC as bidirectional current pulses.

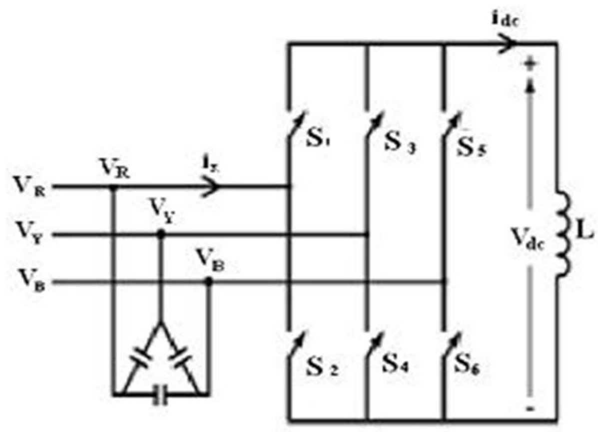

Fig 1. Basic circuit of CSC

A three phase low pass input filter is used at the AC side to filter out the higher order harmonic components of the converter. Nearly sinusoidal line current is obtained with harmonic standards.

III. Distribution Type Staic Synchronous Compensator

STATCOM installed in distribution side of a power system network or nearer to the load terminal to improve the power factor value and the voltage regulation is named as D-STATCOM [6]. D-STATCOMs have faster response and applicable to medium power system networks up to 5MVAr.

Due to the rapidly varying reactive current demand at the utility side of transmission and distribution network, the terminal is protected by the proposed D-STATCOM from voltage sags or flicker. In utility applications, the proposed D-STATCOM provides leading or lagging reactive power to achieve the system stability during the transient.

The proposed current source converter based D-STATCOM regulates the line current flow to the distribution network through a standard power distribution transformer. The STATCOM is designed to generate continuously

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variable inductive or capacitive shunt compensation to the maximum MVA rating of the system. The proposed STATCOM checks the line waveform continuously and compares the deviation with a reference ac signal. So, it provides accurate amount of leading or lagging reactive current compensation and reduce the significant value of voltage fluctuations. DC capacitor, inverter modules, ac filter, coupling transformer and a PWM controller are the main components of a D-STATCOM shown in Fig. 2. The current source inverter of the D-STATCOM converts a dc voltage into a three-phase ac current. AC current output of the inverter is coupled with the ac line through a small tie reactor and ac filter through the synchronization process.

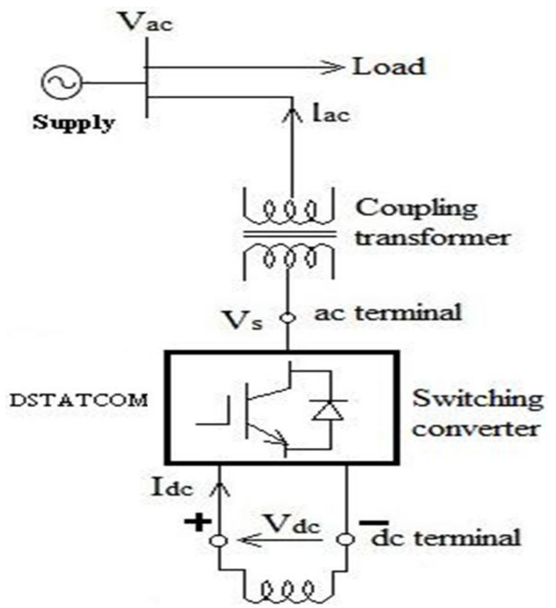

Fig 2. Schematic representation of D-STATCOM

IV. CSC Based D-Statcom

The proposed circuit includes current source converter, dc link reactor, coupling transformer and input filter. The proposed CSC based D-STATCOM is shown in Fig. 3. Design of dc link reactor, types of power semiconductors, design of input filter and control strategy of power semiconductors with PWM technique resolves the designing procedure for power stage of CSC [7].

A. DC Link Reactor

The reactive power (Q) generated by CSC can be expressed as follows

$$Q = \sqrt{\left(\frac{3}{2}\right)}\, VMI_{dc}\cos\theta \qquad (1)$$

The rms value of the generated reactive power is evaluated with the fundamental component of the line-to-line voltage (V) of the converter, modulation index (M), mean dc-link current (I_{dc}) and phase shift angle (è).

Reactive power (Q) generation of the CSC is independent of the dc link inductance. The value of dc link inductance affects the response time of D-STATCOM and the turn off current of the power semiconductor devices leads for the system losses [8]. The applied voltage and current across the dc link inductance is evaluated from the equation 2 and 3 respectively.

$$u_{dc,k}(t) = \left(L_{dc}\frac{d}{dt} + R_{dc}\right) i_{dc,k}(t) \qquad (2)$$

The dc link current of CSC is

$$i_{dc,k}(t) = I_{dco,k}(t) + \frac{u_{dc\,k}(t)}{L_{dc}}\, t \qquad (3)$$

Equation (3) determines the dc link current characteristics. The designed dc link reactor maintains the dc link current i_{dc} as constant.

B. Power Semiconductors selection

The voltage rating to the power semiconductor devices is designed as higher value than the input voltage rating. Maximum acceptable value of the supply voltage at the PCC is also considered to determine the input voltage rating of the CSC. Peak value parameters of the semiconductors during the transient state is considered to determine the maximum controllable turn off current I_T.

C. Design of Input Filter

Low pass filter is designed to filter out the higher order harmonics produced by the converter circuit. The filter circuit sluice the higher order harmonics such as 17th,, 19th, 23rd etc.

The comer frequency rating is designed as low value for the better performance of filtering. This configuration leads

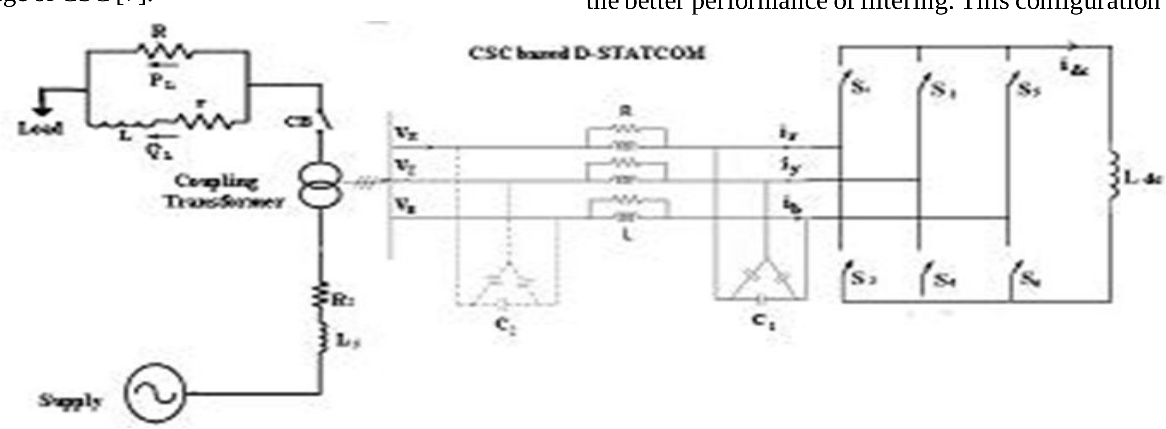

Fig 3. Circuit diagram of CSC based D-STATCOM

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for asymmetrical VAR characteristics [9]. The proposed CSC based STATCOM acts as a fixed capacitive for VAR generation. This concept gives better result in small rating of STATCOM and performs symmetrical compensation in the load terminal by injecting the VAR demand to the circuit. For a maximum rating of STATCOM this method is not effective [3].

A higher rating of series inductance is chosen to eliminate this drawback and implemented in the proposed method. So the shunt capacitor rating is reduced and also maintains the comer frequency as constant. The inductance of the filter circuit is designed properly to avoid undesirable rise of the line to line voltage at the input terminal of the converter.

D. Control method

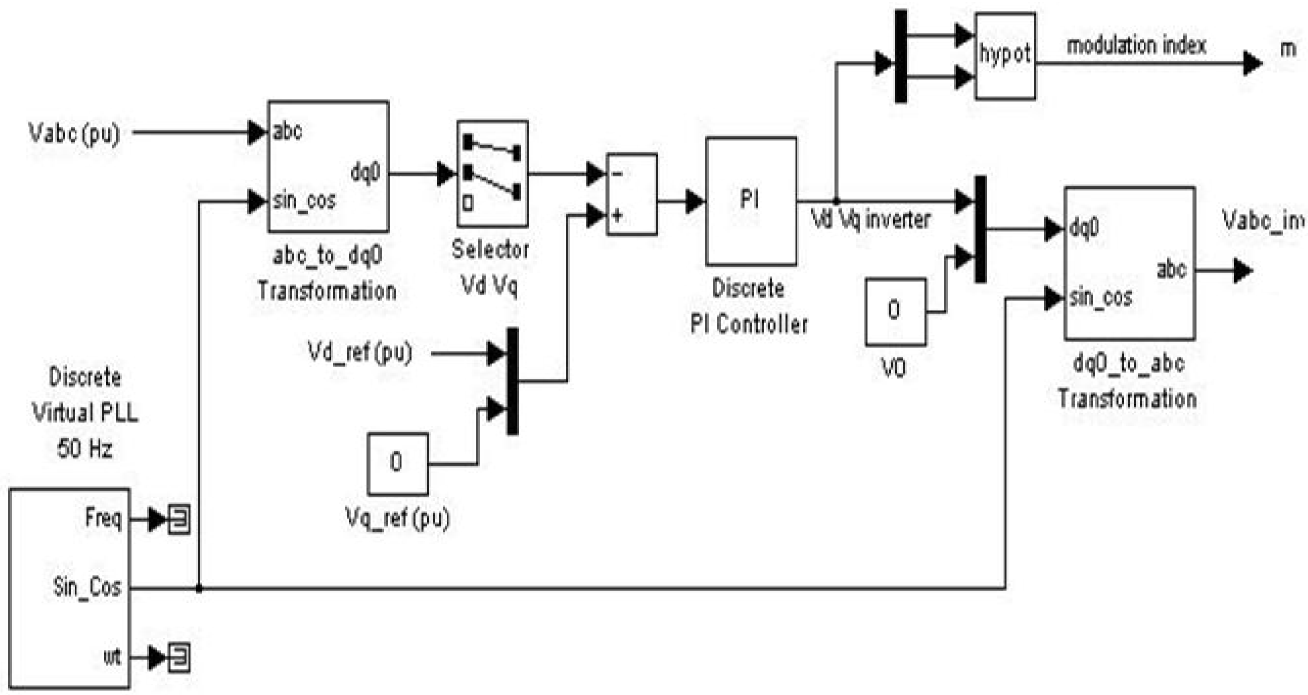

Fig 4. Control system for gate pulse generation

The control diagram of the proposed method is shown in fig. 4. The concept of abc to dqo and dqo to abc transformation is employed to generate the control signal by the control circuit.

For generating sine and cos function of è, discrete PLL block is implemented. Dc voltage reference signal is compared with the dq coordinates for producing the error signal. PI controller is used for controlling the circuit parameters with respect to the generated error signal. A discrete pulse generator is designed to generate the gate signals to converter circuit.

V. Simulation Results

The proposed CSC based D-STATCOM is implemented for the voltage sag compensation by the techniques of harmonic filtering and load balancing. The Simulink model of CSC based D-STATCOM is shown in figure 5.

The current source converter based D-STATCOM is connected in shunt with transmission line. The sag is created in the load terminal at 0.3 sec by closing a switch S1 to include an additional load with the present load. The generated voltage sag is extended up to 0.5 sec.

During the period 0.3S to 0.5S, the load voltage is increased by closing S1. Fig. 6. Shows the Sag created in the output voltage without CSC based D-STATCOM from 0.3S to 0.5S.

The proposed CSC based D-STATCOM with the inductance value of 2.5 mH is connected with the disturbed system and the sag in the output voltage is compensated during the period 0.3S to 0.5S. The compensated output voltage is shown in fig. 8.

Fig. 9 shows the output voltage of the voltage disturbed system after the proposed CSC based D-STATCOM with inductance value varied to 3.0 mH. During the disturbance period , 0.98 p.u value of voltage is constantly maintained by CSC based D-STATCOM.

Fig. 7 shows the output voltage of the voltage disturbed system after the proposed VSC based D-STATCOM with capacitance value of 650uF. During the disturbance period, 0.92 p.u value of voltage is constantly maintained VSC based D-STATCOM.

Above discussion shows, the proposed CSC based D-STATCOM gives better voltage sag mitigation against VSC based D-STATCOM.

Comparison between the CSC based D-STATCOM and VSC based D-STATCOM with respect to the output voltage is shown in Table I and with respect to the design parameters is shown in Table II.

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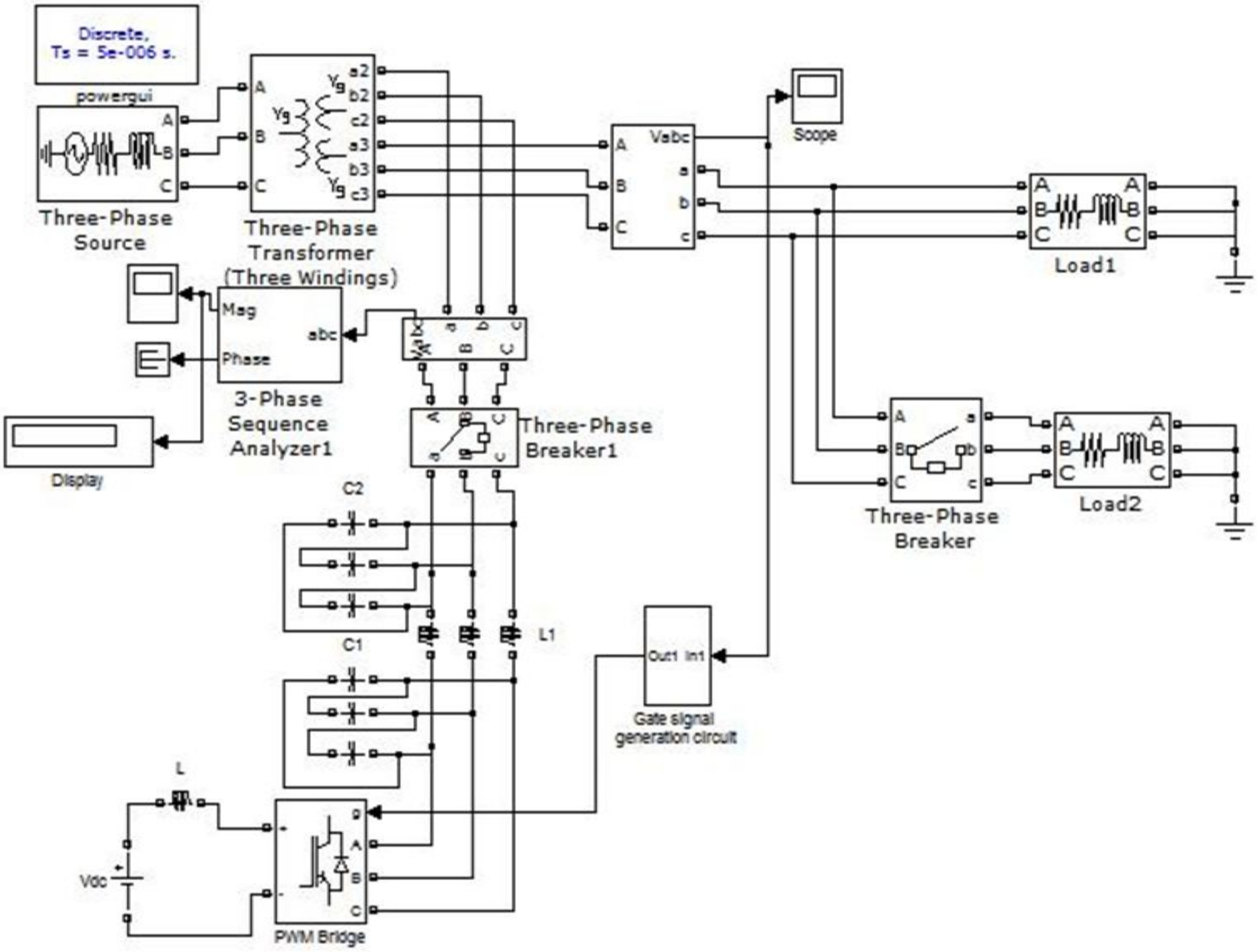

Fig 5. MATLAB simulation model of CSC based D-STATCOM

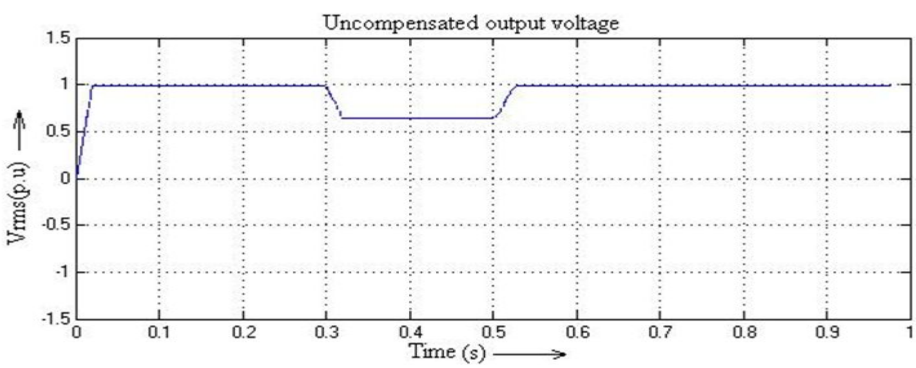

Fig 6. Voltage response of the circuit without CSC based D-STATCOM

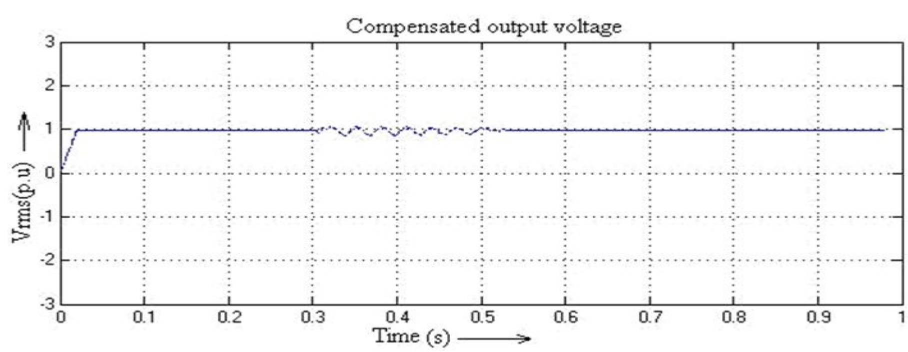

Fig 7. Voltage response of the circuit with VSCbased D-STATCOM

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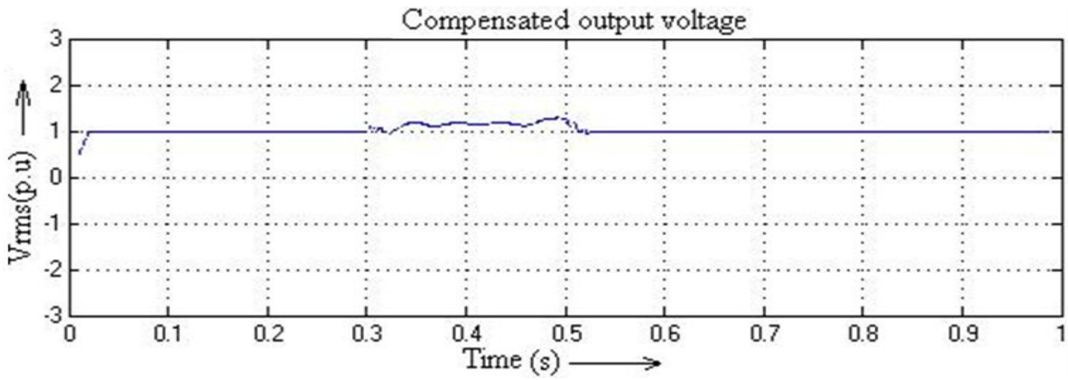

Fig 8. Voltage response of the circuit with CSC based D-STATCOM with L= 2.5 mH

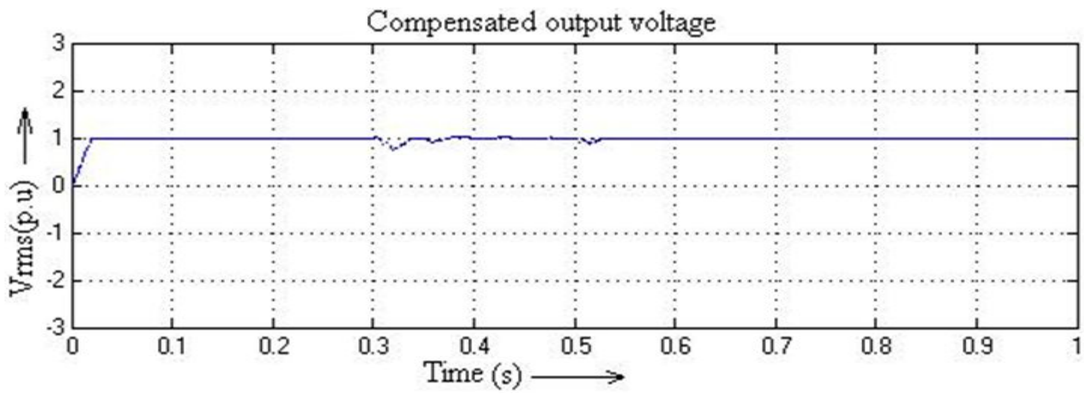

Fig 9. Voltage response of the circuit with CSC based D-STATCOM with L=3mH

TABLE I. DESIGN SPECIFICATIONS FOR VSC AND CSC BASED D- STATCOM

Output Voltage (P.U)	Simulation Period (Sec) 0.1 to 0.3	0.3 to 0.5	0.5 to 1.0
Without controller	1	0.6	1
With VSC based D-STATCOM	1	0.92	1
With CSC based D-STATCOM	1	0.98	1

TABLE II. DESIGN SPECIFICATIONS FOR VSC AND CSC BASED D-STATCOM

Design parameters	VSC based D-STATCOM	CSC based D-STATCOM
DC Supply	15KV	15KV
DC Link	Capacitance = 650uF	Inductance = 3mH
AC side filter parameters	L = 1450uH, C1 = 950uF	L1 = 1450uH, C1 = 950uF, C2 = 1430uF

VI.CONCLUSION

This paper discusses an effective method to overcome the problem of voltage sag mitigation in the utility connected systems with current source converter based D-STATCOM. The voltage sag compensation is achieved effectively in the test system and the results are validated with the simulated output. The proposed technique for voltage sag mitigation gives better result than the VSC based D-STATCOM.

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